UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/028,705	12/28/2001	Myoung Goo Lee	0630-1296P	3917

2292 7590 03/19/2004

BIRCH STEWART KOLASCH & BIRCH
PO BOX 747
FALLS CHURCH, VA 22040-0747

EXAMINER	
KITOV, ZEEV	

ART UNIT	PAPER NUMBER
2836	

DATE MAILED: 03/19/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/028,705	LEE ET AL.	
	Examiner	Art Unit	
	Zeev Kitov	2836	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 January 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 - 18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *7 and 12* is/are allowed.

6)☒ Claim(s) *1 - 6, 8 - 11, 13 - 18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *28 December 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Examiner acknowledges a submission of the amendment and arguments filed on January 21, 2004. Claims 1, 8, 9, 14 and 16 are amended. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action.

1. Drawings

1. The Drawing objection indicated in the first Office Action is withdrawn.

2. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, at least two diodes connected in parallel recited in Claims 14 and 18 must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

2. Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

1. Claims 1, 3 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Avery et al. (US 6,501,632) in a view of Miller et al. (US 5,946,177). Regarding Claim 1, Avery et al. disclose most of the elements of the claim including an electrostatic discharge (ESD) protection circuit having an NMOS transistor connected between an input/output pad and a ground (element NMOS in Fig. 3), the NMOS transistor having a parasitic bipolar transistor (element NPN in Fig. 3); and at least one diode connected between the input/output pad and the NMOS transistor (element Z3 in Fig. 3, col. 2, lines 44 – 67, col. 3, lines 1 - 10). However, it does not disclose the diode with cathode connected to the ground. Miller et al. disclose the diode string (element 327 in Fig. 7) with the cathode of the bottom diode connected to the ground (col. 9, line 33 – col. 10, line 35). Both references have the same problem solving area, namely providing ESD protection for the semiconductor circuits. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the Avery solution by replacing the zener diode by the diode string according to Miller et al, because as Miller et al. state (col. 10, lines 1 – 4), such structure would allow setting a proper firing threshold by selecting a number of diodes.

Regarding Claim 3, Avery et al. disclose the diode as a PN diode (element Z3 in Fig. 3).

Regarding Claim 17, Avery discloses the diode connected between the input /output pad and a substrate of NMOS transistor (element Z1 in Fig. 3) and parasitic bipolar transistor (element NPN in Fig. 3), while Miller et al. discloses a plurality of N diodes connected in series. It further discloses the p-type substrate (shown in Fig. 4)

connected to the ground. A motivation for modification of the primary reference is the same as above.

2. Claims 2, 4 - 6, 8 - 11 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Avery et al. (US 6,501,632) in a view of Miller and further in a view of Menon et al. (US 4,795,918). As was stated above, Avery et al. and Miller et al. disclose all the elements of Claim 1. However, regarding Claim 2, they do not disclose a diode being connected in specific polarity, namely by its cathode to the base of the transistor. Menon et al. disclose a bipolar transistor having a diode connected to the transistor base by its output terminal (cathode) (elements 40 in Fig. 2, col. 3, lines 28 – 38). Both patents have the same problem solving area, namely providing the bipolar transistor with a bias through forward biased diodes. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the Avery et al. solution and replacing the zener diode by the forward biased diodes according to Menon et al., because it is well known in the art, that the zener diode and a group of forward biased diodes are interchangeable and that selection of particular solution is up to designer according to his secondary considerations, such as for example, thermal stability. The forward biased diodes are widely used in the design of band-gap reference voltage sources.

Regarding Claim 4, both Menon et al. and Miller et al. disclose at least one diode as a plurality of PN diodes. The motivation for modification of the primary sources is the same as above.

Regarding Claim 5, Avery et al. disclose that the zener diode is selected so as to stop a current flow through the at least one diode during a normal operation of a chip (col. 3, lines 20 – 5). Accordingly, the amount of forward biased diodes in the Avery et al. structure modified according to Menon et al. is selected the same way.

Regarding Claim 6, both Menon et al. and Miller et al. disclose the plurality of N diodes connected in series to each other in a forward direction (elements 40 in Fig. 2, col. 3, lines 28 – 38 of Menon,) (element 327 in Fig. 7of Miller). The motivation for modification of the primary source is the same as above.

Regarding Claim 8, Avery et al. disclose an electrostatic discharge protection circuit having an input/output pad (element 302 in Fig. 3) and the NMOS transistor (element NMOS in Fig. 3) connected between the input/output pad and having a parasitic bipolar transistor (element NPN in Fig. 3) connected to the zener diode (element Z3 in Fig. 3). Avery et al. further disclose the zener diode Z3 connected between the input/output pad and a high voltage p-well (element HVPW in Fig. 4), which is an extension of a p-substrate of an NMOS transistor; and the NMOS transistor as being connected between the input/output pad and having a parasitic bipolar transistor connected to the zener diode Z3. As to replacement of the zener diode by the plurality of N diodes, Menon et al disclose it. The replacement was discussed above. Regarding at least one diode connected to a ground, both Miller et al. (elements 327 and 326 in Fig. 7 of Miller) and Menon et al. (elements 40 and 42 in Fig. 2 of Menon) disclose at least one of the diodes connected to the ground through resistance. The motivation for modification of primary reference is the same as above.

Regarding Claim 9, Avery discloses the p-type substrate (shown in Fig. 4) connected to the ground.

Regarding Claim 10, both Menon et al. (elements 40 in Fig. 3) and Miller et al. (element 327 in Fig. 7) disclose the plurality of PN diodes. The motivation for modification of the primary source is the same as above.

Regarding Claim 11, Avery et al. disclose that the zener diode is selected so as to stop a current flow through the at least one diode during a normal operation of a chip (col. 3, lines 20 – 5). Accordingly, the amount of forward biased diodes in the Avery et al. structure modified according Miller et al. is selected the same way.

Regarding Claim 13, Avery et al. disclose the circuit, wherein the anode of the zener diode is connected to the base of the parasitic bipolar transistor (elements Z3 and NPN in Fig. 3). As was explained above, the Menon et al. reference provides a solution for modification of the Avery et al. circuit replacing the zener diode by the plurality of N diodes connected to the base of the parasitic bipolar transistor. The motivation for modification of the primary source is the same as above.

3. Claims 14 - 16 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Avery et al in a view of Miller et al. and Menon et al. and further in a view of Duvvury et al. (5,814,865). Regarding Claim 14, Avery et al. disclose an electrostatic discharge (ESD) protection circuit having an input/output pad (element 302 in Fig. 3), and the (zener) diode connected between the input/output pad and a high voltage p-well (element HVPW in Fig. 3), which is an extension of the substrate of an

NMOS transistor, and the NMOS transistor connected between the input/output pad and having a parasitic bipolar transistor connected to the (zener) diode. Menon et al. disclose the plurality of N diodes. However, they neither disclose the plurality of N diodes connected to the base of the bipolar transistor, nor at least two diodes connected in parallel. The plurality of N diodes connected to the base of the bipolar transistor as disclosed by Menon et al. and appropriate motivation for modification of the primary reference was discussed above. As to diodes connected in parallel, these elements are disclosed by Duvvuri et al. (US 5,814,865) (Fig. 2 and 2a, col. 4, lines 9 –37). Both patents have the same problem solving area, namely ESD protection of electronic circuits. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the Avery et al. circuit according to the Duvvury et al., because as Duvvury et al. state (col. 4, lines 9 –37), since the two diodes are in parallel, they, as a pair, will have a lower resistance.

Regarding Claim 15, Avery discloses the p-type substrate (shown in Fig. 4) connected to the ground.

Regarding Claim 16, Menon et al. discloses the diodes as PN diodes. The motivation for modification of the primary source is the same as above.

Regarding Claim 18, Avery discloses the p-type substrate connected to the ground.

3. *Allowable Subject Matter*

Claims 7 and 12 are allowed. A reason for that is that the claim recites, inter alia, connection of the last n+ junction to the substrate, the feature, which was not found in the collected prior art of the record.

4. Response to Argument

An Applicant in his Remarks asked for withdrawal of objections to the Drawings and Oath/Declaration. Both Objections are withdrawn.

As to complaint of the Applicant about not receiving a Notice of Draftperson's Patent Review PTO-948, the Examiner approved the Drawings, which was indicated in the form PTO-326 attached to the First Action.

As to remarks regarding art rejections, the Applicant's amendment necessitated the new ground of rejection. Therefore Applicant's remarks are moot in a view of that.

However, one of them needs to be discussed. Examiner disagrees with the Applicant's argument that Menon et al. reference (and Miller et al. in the second Office Action) fail to disclose "a diode or diode-connected transistor having a cathode thereof actually connected to the ground". The Menon et al. reference (and Miller et al. also) disclose the diode or diode-connected transistor having a cathode connected to the ground through additional resistor (element 42 in Fig. 2 of Menon and element 326 in Fig. 7 of Miller). The Applicant may argue that this is not direct connection (a meaning of word "actually" in his arguments is not clear). However in such case, the counter-argument will be that the Applicant himself does not disclose the direct connection of

the diode cathode to the ground, but only through the substrate. The direct connection of the diode cathode to the ground would short circuit a control terminal of the transistor, thus making the circuit inoperable. Therefore, both references satisfy the claim limitations of the diode cathode connection to the ground.

5. Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Zeev Kitov whose current telephone number is (571) 272 - 2052. The examiner can normally be reached on 8:00 – 4:30. If attempts to reach examiner by telephone are unsuccessful, the examiner's supervisor, Brian Sircus can be reached on (571) 272 – 2800, Ext. 36. The fax phone number for organization where this application or proceedings is assigned is (703) 872-9306 for all communications.

Z.K.
03/10/2004

GREGORY J. TOATLEY, JR.
PRIMARY EXAMINER